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ABSTRACT

A β-Ga_2O_3 field effect transistor (FET) outperforms a GaN FET in Baliga's figure of merit (FOM) by 400% and Huang's chip area manufacturing figure of merit by 330%, suggesting that β-Ga_2O_3 could be a substrate of choice for next generation power transistors. However, its low thermal conductivity leads to extreme self-heating, which deteriorates the device performance during high voltage operation. A holistic evaluation of performance from a material-device-circuit perspective is necessary before reaching any conclusion regarding the technological viability of β-Ga_2O_3. In this paper, we develop a multiphysics and multiscale model for a material-device-circuit analysis of β-Ga_2O_3 FETs. The framework allows us to explore the effectiveness of various device design strategies (e.g., thermal shunts) for mitigating the thermal chokepoints and compare the performance of improved β-Ga_2O_3 FETs against that of GaN and SiC FETs. We highlight the limitations of traditional FOMs to analyze the relative performance of the new generation of power transistors whose structure incorporates stacked layers of materials with different thermal conductivities, like those of β-Ga_2O_3 FETs. We suggest device design strategies, such as wafer thinning, incorporation of heat shunts, and improved channel mobility, so that β-Ga_2O_3 FETs can compete commercially with GaN and SiC technologies.

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β-Ga_2O_3 is often mentioned as a low-cost and high-performance next generation channel material for power transistors because it outperforms traditional GaN and SiC substrates in terms of Baliga and Huang electrical figures of merit (FOMs). Indeed, KV-class Schottky barrier diodes[1] and high-voltage lateral field effect transistors (FETs)[2] have already been demonstrated. However, there is a persistent concern that the self-heating associated with the low-thermal conductivity β-Ga_2O_3 ($\lambda \sim$ 10–25 W/m K)[3] may compromise its electrical performance and prevent its widespread adoption. In fact, β-Ga_2O_3 is far inferior to GaN in terms of electrothermal metrics: by 900% in terms of Keyes figure of merit[4] $\{\lambda[(c.V_s)/(4\pi\varepsilon)]^{0.5}\}$ and by 2300% in terms of Huang's thermal figure of merit[5] $(\lambda/\varepsilon E_c)$. This challenge of self-heating is well known, and one of the solutions includes high-λ substrates [e.g., sapphire,[6] diamond,[3] and silicon carbide (SiC)[7]] to reduce self-heating and improve on-current. An integrated device-circuit-system simulation is necessary to see if this strategy would actually help β-Ga_2O_3 achieve performance comparable to GaN and SiC.

Experimentally calibrated, self-consistent device and circuit simulations by technology computer-aided design (TCAD) and HSPICE models allow one to accurately predict system performances under a variety of operating conditions, identify performance bottlenecks, and suggest routes to application-specific optimization. Existing TCAD models[8] do not explicitly account for self-heating effects (SHEs) of β-Ga_2O_3 transistors. They cannot, therefore, predict the circuit performance of the transistor for application-specific, high-voltage, and high-temperature operation. In this letter, we develop a self-consistent TCAD model calibrated with experimental data, which can predict the output and transfer characteristics of β-Ga_2O_3 FETs including SHE effects. To account for the SHE, we first calculate the thermal resistance R_{th} and thermal capacitance C_{th} of the specific transistor geometry by solving the heat-diffusion equation. The thermal-RC network is then embedded in a self-consistent electrothermal HSPICE model. We use the model to analyze, as an illustrative example, the performance of β-Ga_2O_3 FETs in a boost converter. This versatile model allows us to explore a variety of device structures to reduce R_{th} and to see if indeed the suggested redesign would improve the performance of β-Ga_2O_3 FETs.

We have developed a TCAD model using the commercial device simulator Sentaurus from Synopsis.[9] This electrothermal simulator self-consistently solves for position-resolved electron and hole concentrations and the lattice temperature. For electrical simulation, a key challenge is the temperature dependence of mobility associated with the complex band structure of β-Ga_2O_3. We adopted the analytical power-law mobility model with empirical fitting parameters to

approximate the mobility between 300 and 500 K.[10] Other device parameters (e.g., doping density $2.7 \times 10^{18}/\mathrm{cm}^3$) are summarized in the caption of Fig. 1. Thermal modeling of a power transistor poses additional challenges. While electrical transport is confined to the thin β-Ga_2O_3 layer, the self-heating of the channel is defined by the thermal conductivity (λ) and the dimensions of both the channel and the substrate. To calibrate against experimental data,[3,6] we assumed that the β-Ga_2O_3 device rests on a substrate 500 μm thick and 200 μm wide (increasing the width further does not affect the results). Figure 1 shows the multilayer device stack necessary for the accurate thermal modeling of the transistors, with layer thicknesses varying from a few nanometers to hundreds of micrometers. The source, gate, drain and substrate contacts act as heat sinks.

The coupled electrothermal model was used to calculate output and transfer characteristics of this depletion-mode transistor, and the results were validated against experimental data from β-Ga_2O_3 FETs with three different substrates (e.g., diamond, sapphire, and silicon on insulator, SOI), as shown in Fig. 2. The multiple-substrate validation ensures that the thermal model and the electron-hole transport models are independently calibrated. The deviation between experimental data and the model prediction in the linear region is explained by the fact that the idealized device considered in the simulation does not account for the series resistance. Indeed, contact engineering to reduce specific on-resistance remains an important research topic for β-Ga_2O_3 transistors. In the context of this paper, the maximum self-heating is defined by the saturation characteristics, which is well described by device simulation.

For additional and independent validation of the thermal model, we compared the junction temperature predicted by the TCAD model with the position-resolved surface-temperature from the thermoreflectance (TR) measurement (see the supplementary material). The comparison is meaningful because most of the heat generation within the FET occurs in the thin channel lying very close to the surface. Figure 3(e) shows that the junction temperature rise (ΔT), when plotted with power ($P = V_{DS} \times I_D$) normalized by the area, replicates the experimental data accurately. The temperature profiles ($V_{GS} = -8$ V;

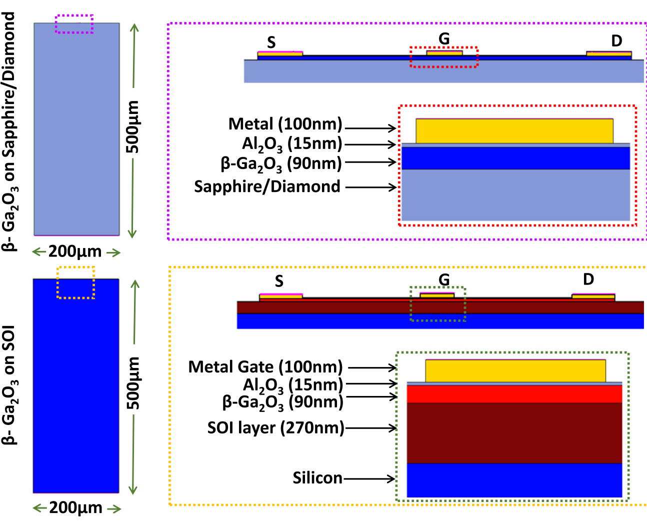

FIG. 1. Device structures in the Synopsis™ TCAD simulator. The dimensions of the device are taken from the fabricated devices.[3,6] The substrate was considered to be n-doped with a concentration of $2.7 \times 10^{18}/\mathrm{cm}^3$. The low field electron mobilities were determined by fitting the experimental I–V characteristics. They were found to be 49, 36, and 23 cm^2/V s in the case of diamond, sapphire, and SOI substrates, respectively. S, G, and D represent the source, gate, and drain, respectively.

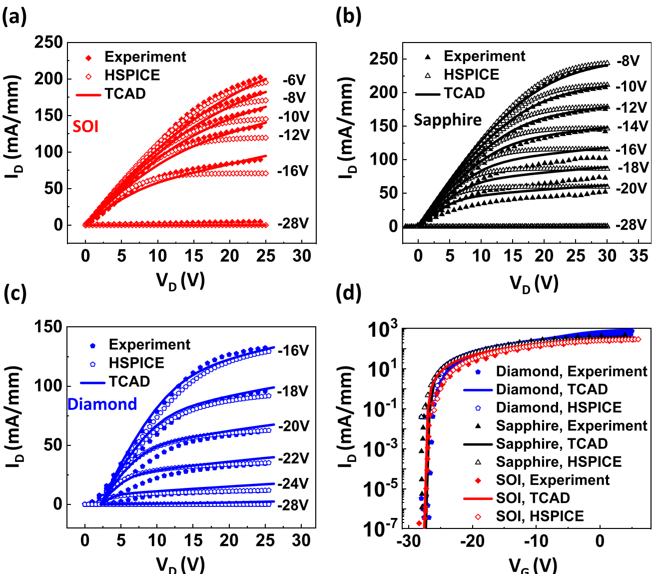

FIG. 2. Output characteristics obtained from experiments, TCAD and HSPICE compact model for (a) SOI, (b) sapphire, and (c) diamond. (d) Transfer characteristics of β-Ga_2O_3 FETs on the three substrates and TCAD and HSPICE outputs. The TCAD and HSPICE modes reproduce the experimental data accurately.

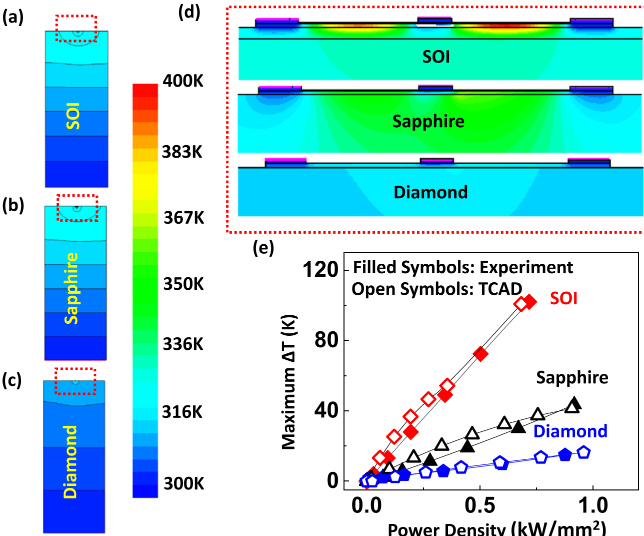

FIG. 3. Temperature profiles obtained from TCAD at $V_{DS} = 30$ V and $V_{GS} = -8$ V for β-Ga_2O_3 FETs on (a) SOI, (b) sapphire, and (d) diamond. The dimensions of the devices are given in Fig. 1. (d) The temperature of the FET on different substrates, viz., SOI, sapphire, and diamond. (e) Maximum temperature rise (ΔT) in the devices from the TCAD model reproduces the experimental thermoreflectance data accurately. The filled symbols are experimental data, and open symbols are TCAD data.

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$V_{DS} = 30$ V) of the β-Ga_2O_3 FETs on three substrates show the dramatic position-resolved temperature rise when the transistor operates with a low λ substrate, SOI. The temperatures recorded using the TR measurement are little lower than those of TCAD simulation, possibly because we did not account for the convective loss from the surface of the transistor. Given the well-calibrated 3D electrothermal TCAD model for β-Ga_2O_3 transistors, we now need to determine the performance of various circuits based on this transistor technology. Toward the goal of quantifying the efficiency loss due to self-heating, we will first need to develop a compact electrothermal model as discussed next.

A β-Ga_2O_3 compact model was developed by adapting and generalizing the MIT Virtual Source GaNFET-HV SPICE Model[11] for the relevant device physics, parameters, and dimensions. The mobility values obtained from TCAD were used for the corresponding devices. In particular, unlike classical transistors, the compact model includes two self-consistent subcircuits for electrical and thermal responses. We evaluated the thermal resistance for all three substrates, viz., diamond, sapphire, and SOI, by solving the Fourier equation for heat-conduction by using the COMSOL Multiphysics software.[12] The thermal capacitance was obtained from device dimensions and further refined during calibration with experimental transfer and output characteristics. The compact model reproduces the experimental data well, as seen from Fig. 2. This well-calibrated electrothermal HSPICE compact model can now be used to analyze the circuit performance of β-Ga_2O_3 FETs.

To quantify the implications of self-heating associated with a β-Ga_2O_3 technology, we chose to analyze the performance of a boost converter circuit, see Fig. 4(a). The boost converter circuit is widely used as a dc/dc converter in power electronic systems and finds applications in sensors, portable speakers, USB chargers, etc. It is important to realize that the FET dimensions necessary for use in the boost converter circuit are much larger than those of the devices used for model calibration (i.e., Figs. 1 and 2). Therefore, the thermal parameters ($\boldsymbol{R_{th}}$, $\boldsymbol{C_{th}}$) of the new device geometry were recalculated from the COMSOL simulator. The electrical and thermal simulations used identical device geometry (i.e., 200×500 μm^2, see Fig. 1). The β-Ga_2O_3 layer is 8 μm long, and the 1 μm heat source close to the drain emulates the region of power dissipation for the transistor. The thermal properties and thicknesses of various layers in the substrate are summarized in the supplementary material. The thermal resistance was calculated with the following boundary conditions: $\Delta T_b = 0$ K at the bottom surface and insulating (zero-flux) boundary condition for the remaining surfaces (except the heat source). The boundary condition implies that convective heat loss is negligible. The initial condition was set at $\Delta T = 0$ K for the whole structure. A power of 1 W was applied to the structure, and the thermal resistance was obtained by recording the maximum temperature rise ($R_{TH} = \Delta T_{max}/P$). Finally, we used a FET with threshold voltage, $V_{th} = -4$ V (corresponding to the β-Ga_2O_3 layer thickness of 20 nm[13]), for all the simulations. We do realize that in practice enhancement mode, FETs are preferred because depletion mode FETs with negative threshold voltage (V_{th}) require a complex gate drive circuit for fail-safe operation.[8] The existing technology is further developed so that it can support enhancement mode operation with sufficient drive current, which will be an important topic for future research.

For a fair comparison of performances among the β-Ga_2O_3 FET on three substrates, we need to determine the best possible operating conditions for the boost converter. Since the β-Ga_2O_3 FET needs to be turned off and on periodically, we chose our driving clock to have a lower limit of -10 V and a higher limit of 0 V, keeping the chosen V_{th} well within the operating voltage limits and giving the FETs a reasonably good operating range. To determine the duty cycle for the operations, we investigate the conversion ratio (V_{out}/V_{in}) and efficiency ($\eta = P_{out}/P_{in}$) subjected to various duty cycles (%), as shown in Fig. 4(b). In order to have both high enough efficiency and conversion ratio, a duty cycle of 30% was chosen for all the simulations. Other circuit parameters are summarized in the caption of Fig. 4.

The efficiency of the boost converter is influenced directly by the output current, which is in turn determined by the degree of self-heating in the device. From Fig. 5(b), we found that the β-Ga_2O_3 FET on SOI has an efficiency of 81.6% at 250 kHz, which decreases rapidly at higher frequencies. The SOI substrate has very severe heating, which results in lower inductor current (I_L) as shown in Fig. 5(a), and eventually very low efficiency. The FETs on sapphire and diamond have lower self-heating and therefore higher efficiency (89% and 91%, respectively, at 250 kHz) but cannot match the efficiencies of GaN FET[14] or SiC FET[15] (>95%) boost converters. Therefore, although theoretically β-Ga_2O_3 has low parasitic capacitances for the same on-resistance and a much lower switching loss compared to a SiC or a

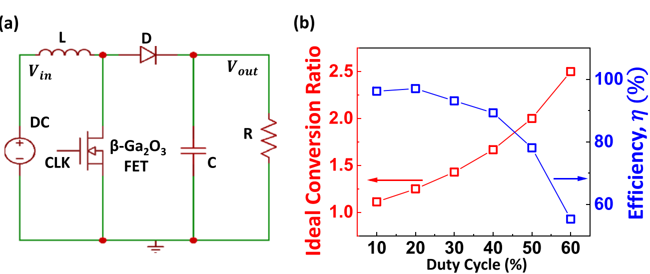

FIG. 4. (a) The boost converter circuit used in our analysis. Circuit parameters: Inductor, L = 3000 μH, FET = β-Ga_2O_3 on SOI/sapphire/diamond, capacitance, C = 50 μF, D = diode, load resistance, R = 2000 Ω, $\boldsymbol{V_{in}}$ = input voltage, and $\boldsymbol{V_{out}}$ = output voltage. For the diode, SBR3U100LP with a forward voltage drop, $V_F = 0.79$ V, and total capacitance, $C_T = 800$ pF, has been used. (b) Ideal conversion ratio and efficiency vs duty cycle of the boost converter circuit.

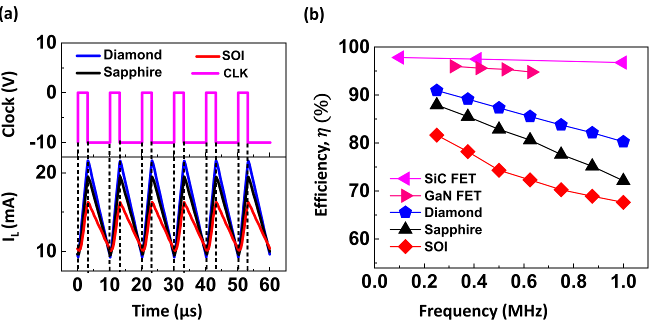

FIG. 5. (a) Inductor current ($\boldsymbol{I_L}$) of the boost converter circuit. The clock input is with a 30% duty cycle, and the driving voltage is from 0 to -10 V. (b) Efficiency of the circuit with a SiC FET,[14] GaN FET,[15] β-Ga_2O_3 FET on diamond (500 μm) FET,[3] sapphire (500 μm),[6] and SOI (270 nm/500 μm).[6]

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GaN FET, β-Ga_2O_3 FETs suffer from severe self-heating, which makes the technology inferior to its competitors even though expensive bulk substrates (e.g., sapphire and diamond) are used. Even a more advanced thermal substrate involving heat shunts does not offer significant improvement. For example, several groups have recently suggested the use of a thin layer of very high thermal conductivity substrates [e.g., hexagonal boron nitride (hBN) ($\lambda = \sim600$ W/m K)[16] or aluminum nitride (AlN)][17] as interfacial thermal shunt, but the efficiency is still lower than that of typical GaN FETs.[13] Therefore, the key conclusion of this section is that despite remarkable performance, the devices reported in the literature may still not be sufficiently efficient for practical power electronics applications.

An interesting observation regarding the transistor performance discussed above is this: While the β-Ga_2O_3 FET performance is indeed inferior to that of SiC or GaN FETs, it is not neither as poor as classical Keyes/Huang FOMs may suggest, nor as good as the Baliga FOM[18] may imply. Moreover, none of the existing FOMs anticipate the substrate dependence of transistor performance. Indeed, several limitations of the existing FOMs make the performance evaluation of β-Ga_2O_3 FETs difficult. The Baliga FOM considers only conduction losses but ignores switching losses.[5] The Baliga high frequency figure of merit[19] includes switching losses; however, it can only be used to compare device performances once $R_{on,sp}$ and $C_{in,sp}$ are known.[5] They both emphasize the importance of the large bandgap, without accounting for the corresponding thermal conductivity. It is easy to understand why these FOMs overestimate the performance of semiconductors with poor thermal conductivity.

In contrast, Keyes' and Huang's FOMs do account for the thermal conductivity of the semiconductor, but they give the same values for β-Ga_2O_3 FETs, irrespective of whether the substrate is native β-Ga_2O_3, SOI, sapphire, or diamond. Moreover, GaN and SiC technologies are often build onto host substrates not accounted for in the classical FOM. We conclude that the FOM should replace λ of the channel material with λ_{eff} that accounts for the thermal-resistance of the whole device.

The self-heating limited performance of β-Ga_2O_3 transistors in power-electronics systems, despite the use of high λ substrates, comes as a surprise. The conclusion reflects the use of relatively thick ($\sim$500 μm) substrates in the literature. Both the device and circuit performance can be improved if the substrate is thinned. In this regard, a particularly promising approach involves β-Ga_2O_3 transistors fabricated on a stack of tens of nm thick h-BN[13] on the 100 μm thick silicon substrate (see the supplementary material). The high bandgap of h-BN serves as a tunneling barrier as well as a high thermal conductivity heat shunt.

Therefore, despite the promising experimental demonstrations of a variety of power devices, we determine that the low-λ will hinder the commercial adoption of β-Ga_2O_3 FETs for power electronics applications. The device-circuit models presented in the paper quantify the detrimental effect of severe self-heating, even in the case of high λ substrates like sapphire and diamond. The various device configurations existing currently in the literature do not provide much improvement. Based on the analysis presented in this paper, we conclude that only a combination of improved channel mobility, high thermal conductivity heat shunts, and wafer thinning (see the supplementary material) will make β-Ga_2O_3 FETs commercially competitive to GaN or SiC FETs.

See the supplementary material for the details of thermal simulation in COMSOL, thermoreflectance imaging, and simulations for potential performance improvement of β-Ga_2O_3 FETs.

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The authors declare no competing financial interest.

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